19. (amended) The apparatus of Claim 6, wherein an instruction set is provided to said first processor, comprising at least one field of execution conditions which is intended therefor and comprises at least the following classes of instructions:

integers corresponding to arithmetic and logic operations on integer numbers;

transfer corresponding to the transfer operations between a register in said protocol processor and memory; and

monitoring corresponding to the monitoring of all of the operations modifying the value of an incrementation register in said first [protocol] processor.

35. (amended) The apparatus of Claim 6, wherein said vector processing includes signal processing tasks generally carried out by a DSP and matrix computation which requires a more powerful structure than that of the DSP and which is generally of the array processor type.[?]

REMARKS

Claims 16 and 18 have been cancelled. Accordingly, the 35 U.S.C. 112, first paragraph, rejections of Claims 16 and 18 and the objection to the drawings under 37 CFR 1.83(a) are moot.

Claims 19 and 35 have been amended better to define the invention and overcome the 35 U.S.C. 112 rejections.

Applicants submit herewith a Terminal Disclaimer to overcome the double-patenting rejection of Claims 36-39.

Claims 6, 14-15 and 17 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama et al. (4,964,035). Applicants respectfully traverse.